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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Steven L. Scott et al.

MULTISTREAM PROCESSING MEMORY-AND BARRIER-SYNCHRONIZATION  
METHOD AND APPARATUS

Docket No.: 1376.733US1  
Filed: August 18, 2003  
Examiner: Unknown

Serial No.: 10/643,741  
Due Date: N/A  
Group Art Unit: 2153

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Information Disclosure Statement (2 pgs.), Form 1449 (4 pgs.), and copies of 47 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
Customer Number 21186

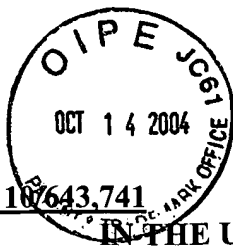
By: Thomas F. Brennan  
Atty: Thomas F. Brennan  
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JAMES KANYUSIK  
Name

James Kanyusik  
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
(GENERAL)



**S/N 10/643,741**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Steven L. Scott et al. Examiner: Unknown  
Serial No.: 10/643,741 Group Art Unit: 2153  
Filed: August 18, 2003 Docket: 1376.733US1  
Title: MULTISTREAM PROCESSING MEMORY-AND BARRIER-  
SYNCHRONIZATION METHOD AND APPARATUS

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**COMMUNICATION CONCERNING RELATED APPLICATIONS**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/643742	August 18, 2003	1376.697US1	DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM
10/643586	August 18, 2003	1376.699US1	DECOUPLED VECTOR ARCHITECTURE
10/643585	August 18, 2003	1376.700US1	LATENCY TOLERANT DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER
08/450251 5721921	May 25, 1995	499.580US1	BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS
08/165265 5434995	December 10, 1993	200.466US1	BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS
08/615671 5835925	March 13, 1996	200.581US1	USING EXTERNAL REGISTERS TO EXTEND MEMORY REFERENCE CAPABILITIES OF A MICROPROCESSOR

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/643,741

Filing Date: August 18, 2003

Title: MULTISTREAM PROCESSING MEMORY-AND BARRIER-SYNCHRONIZATION METHOD AND APPARATUS

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Dkt: 1376.733US1

10/643754	August 18, 2003	1376.724US1	RELAXED MEMORY CONSISTENCY MODEL
10/643758	August 18, 2003	1376.729US1	REMOTE TRANSLATION MECHANISM FOR A MULTINODE SYSTEM

Respectfully submitted,

STEVEN L. SCOTT ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 373-6909

Date October 12, 2004 By Thomas F. Brennan  
Thomas F. Brennan  
Reg. No. 35,075

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JAMES KAWYUSIK  
Name

James Kawyusik  
Signature

S/N 10/643,741



PATENT

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Applicant:	Steven L. Scott et al.	Examiner:	Unknown
Serial No.:	10/643,741	Group Art Unit:	2153
Filed:	August 18, 2003	Docket:	1376.733US1
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**INFORMATION DISCLOSURE STATEMENT**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

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Dkt: 1376.733US1

The present application is a U.S. national patent application filed after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed Telephone number if there are any questions regarding this communication.

Respectfully submitted,

STEVEN L. SCOTT ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
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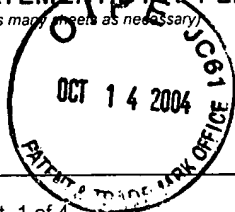
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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 1 of 4

Complete if Known

<b>Application Number</b>	10/643,741
<b>Filing Date</b>	August 18, 2003
<b>First Named Inventor</b>	Scott, Steven
<b>Group Art Unit</b>	2153
<b>Examiner Name</b>	Unknown

Attorney Docket No: 1376.733US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,771,391	09/13/1988	Blasbalg, Herman	364	514	07/21/1986
	US-4,868,818	09/19/1989	Madan, Herb S., et al.	371	11	10/29/1987
	US-4,933,933	06/12/1990	Dally, William J., et al.	370	60	12/19/1986
	US-5,008,882	04/16/1991	Peterson, , et al.	370	943	08/17/1987
	US-5,031,211	07/09/1991	Nagai, Yasuhiro , et al.	379	221	02/01/1990
	US-5,036,459	07/30/1991	Den Haan, Petrus A., et al.	364	200	03/09/1989
	US-5,105,424	04/14/1992	Flaig, Charles M., et al.	370	941	06/02/1988
	US-5,157,692	10/20/1992	Horie, Takeshi , et al.	375	38	03/20/1990
	US-5,161,156	11/03/1992	Baum, Richard I., et al.	371	7	02/02/1990
	US-5,170,482	12/08/1992	Shu, Renben , et al.	395	800	02/13/1991
	US-5,175,733	12/29/1992	Nugent, Steven F.	370	94	12/27/1990
	US-5,218,601	06/08/1993	Chujo, Takafumi , et al.	370	16	12/20/1990
	US-5,218,676	06/08/1993	Ben-ayed, Mondher , et al.	395	200	01/08/1990
	US-5,239,545	08/24/1993	Buchholz, Dale R.	370	95.3	11/05/1990
	US-5,276,899	01/04/1994	Neches, Philip M.	395	800	08/10/1990
	US-5,280,474	01/18/1994	Nickolls, John R., et al.	370	60	01/05/1990
	US-5,313,628	05/17/1994	Mendelsohn, Noah R., et al.	395	575	12/30/1991
	US-5,313,645	05/17/1994	Rolfe, David B.	395	800	05/13/1991
	US-5,331,631	07/19/1994	Teraslinna, Kari T.	370	60	03/16/1993
	US-5,333,279	07/26/1994	Dunning, Dave	395	325	06/01/1992
	US-5,341,504	08/23/1994	Mori, Kinji , et al.	395	800	03/01/1990
	US-5,347,450	09/13/1994	Nugent, Steven F.	395	200	08/19/1993
	US-5,353,283	10/04/1994	Tsuchiya, Paul F.	370	60	05/28/1993
	US-5,365,228	11/15/1994	Childs, Philip L., et al.	340	825.8	08/21/1991
	US-5,434,995	07/18/1995	Oberlin, Steven M., et al.	395	550	12/10/1993
	US-5,440,547	08/08/1995	Easki, Hiroshi , et al.	370	60	01/05/1994
	US-5,517,497	05/14/1996	LeBoudec, Jean-Yves , et al.	370	60.1	03/21/1995
	US-5,546,549	08/13/1996	Barrett, Linda , et al.	395	309	06/01/1994

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DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

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<b>Application Number</b>	10/643,741
<b>Filing Date</b>	August 18, 2003
<b>First Named Inventor</b>	Scott, Steven
<b>Group Art Unit</b>	2153
<b>Examiner Name</b>	Unknown

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Attorney Docket No: 1376.733US1

US-5,548,639	08/20/1996	Ogura, Takao , et al.	379	221	10/22/1992
US-5,550,589	08/27/1996	Shiojiri, Hiroshisa , et al.	348	387	11/04/1994
US-5,555,542	09/10/1996	Ogura, Takao , et al.	370	94.1	01/11/1996
US-RE28,577	10/21/1975	Schmidt, William G.	179	15 BA	11/21/1973

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
	EP-0353819A2	02/07/1990	Gupta, Rajiv , et al.	G06F	9/46	
	EP-0473452A2	03/04/1992	Duerschmid, O. , et al.	G06F	9/46	
	EP-0475282A2	03/18/1992	Kametani, Masatusugu	G06F	9/46	
	EP-0501524A2	09/02/1992	Hillis, Daniel W., et al.	G06F	15/16	
	EP-0570729A2	11/24/1993	Collins, Clive A., et al.	G06F	15/16	
	WO-87/01750A1	03/26/1987	Anderson, S.	E04B	1/94	
	WO-88/08652A1	11/03/1988	Hillis, D. W., et al.	H04J	3/26	
	WO-95/16236A1	06/15/1995	Oberlin, Steven M., et al.	G06F	9/46	
	WO-96/10283A1	04/04/1996	Bonner, J.	H02 H	3/087	
	WO-96/32681A1	10/17/1996	Thorson, Gregory M., et al.	G06F	15/16	

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		"Deadlock-Free Routing Schemes on Multistage Interconnection Networks", IBM Technical Disclosure Bulletin, 35, (December, 1992),232-233	
		ADVE, V. S., et al., "Performance Analysis of Mesh Interconnection Networks with Deterministic Routing", Transactions on Parallel and Distributed Systems, (March 1994),225-246	
		BOLDING, KEVIN , "Non-Uniformities Introduced by Virtual Channel Deadlock Prevention", Technical Report 92-07-07, Department of Computer Science and Engineering, FR-35 University of Washington; Seattle, WA 98195, (July 21, 1992),	
		BOLLA, F R., "A Neural Strategy for Optimal Multiplexing of Circuit and Packet-Switched Traffic", Department of Communications, Computer and Systems Science (DIST), University of Genova, 1324-1330	
		BOURA, Y M., et al., "Efficient Fully Adaptive Wormhole Routing in n-dimensional Meshes", IEEE, (1994),589-596	
		BUNDY, A. , et al., "Turning Eureka Steps into Calculations in Automatic Program", UK IT, (IEE Conf. Pub. 316), (1991),221-226	
		CARLILE, BRADLEY R., "Algorithms and Design: The CRAP APP Shared-Memory System", COMPCON SPRING '93, San Francisco, CA, (February 22, 1993),312-320	

EXAMINER

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		CHIEN, A. A., et al., "Planar-Adaptive Routing: Low-Cost Adaptive Networks for Multiprocessors", <u>Pro. 19th International Symposium on Computer Architecture</u> , (May 1992),268-277	
		DALLY, W. J., et al., "Deadlock-Free Adaptive Routing in Multicomputer Networks Using Virtual Channels", <u>I.E.E.E. Transactions on Parallel and Distributed Systems</u> , 4(4), (April 1993),466-475	
		DALLY, WILLIAM , et al., "Deadlock-Free Message Routing in Multiprocessor Interconnection Networks", <u>IEEE Transactions on Computers</u> , C-36, (May 1987),547-553	
		DALLY, WILLIAM , "Performance Analysis of k-ary n-cube Interconnection Networks", <u>IEEE Transactions on Computers</u> , 39(6), (June 1990),775-785	
		DALLY, W. J., "Virtual Channel Flow Control", <u>Pro. 17th International Symposium on Computer Architecture</u> , pp. 60-68, May 1990,	
		DUATO, J. , "A New Theory of Deadlock-Free Adaptive Routing in Wormhole Networks", <u>I.E.E.E. Transactions on Parallel and Distributed Systems</u> , 4(12), (Dec 1993),1320-1331	
		FAANES, G. J., et al., "DECOUPLED VECTOR ARCHITECTURE", <u>US Patent Application Ser. No. 10/643,586</u> , filed August 18, 2003 (1376.699US1), 47 Pages	
		GALLAGER, ROBERT , "Scale Factors for Distributed Routing Algorithm", <u>NTC '77 Conference Record</u> , 2, at 2-1 through 2-5,	
		GHARACHORLOO, KOUROSH , "Two Techniques to Enhance the Performance of Memory Consistency Models", (1991),	
		GLASS, C. J., et al., "The Turn Model for Adaptive Routing", <u>Pro. 19th International Symposium on Computer architecture</u> , (May 1992),278-287	
		GRAVANO, L , et al., "Adaptive Deadlock- and Livelock-Free Routing with all Minimal Paths in Torus Networks", <u>IEEE Transactions on Parallel and Distributed Systems</u> , 5(12), (December 1994),1233-1251	
		GUPTA, RAJIV , et al., "High speed Synchronization of Processors Using Fuzzy Barriers", <u>International Journal of Parallel Programming</u> 19 (1990) February, No. 1, New York, US pp 53-73,	
		ISHIHATA, HIROAKI , et al., "Architecture of Highly Parallel AP1000 Computer", <u>Scripta Technica, Inc.</u> , Systems and Computers in Japan 24, No. 7,,(1993),pp. 69-76	
		JESSHOPE, C. R., et al., "High Performance Communications in Processor Networks", <u>Proc. 16th International Symposium on Computer Architecture</u> , (May 1989),pgs. 150-157	
		KIRKPATRICK, S. , et al., "Optimization by Simulated Annealing", <u>SCIENCE</u> , May 13, 1993, 220(4599), (May 1983),671-680	

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		LINDER, DANIEL H., et al., "AN ADAPTIVE AND FAULT TOLERANT WORMHOLE ROUTING STRATEGY FOR K-ARY N-CUBES", <u>IEEE TRANSACTIONS ON COMPUTERS</u> , 40(1), (1991), pgs. 2-12	
		LUI, Z, et al., "Grouping Virtual Channels for Deadlock-Free Adaptive Wormhole Routing", <u>PARLE '93 Parallel Parallel Architectures and Languages Europe</u> , 5th International PARLE Conference, Munich, Germany, (June 14-17, 1993), 254-265	
		NUTH, PETER, et al., "The J-Machine Network", <u>IEEE</u> , (1992), pgs. 420-423	
		O'KEEFE, MATTHEW T., et al., "Static Barrier MIMD: Architecture and Performance Analysis", <u>Journal of Parallel and Distributed Computing</u> No. 2, (March 25, 1995), pp. 126-132	
		SCOTT, S. L., "DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM", <u>US Patent Application Ser. 10/643,742</u> , filed August 18, 2003 (1376.697US1), 27 Pages	
		SCOTT, S. L., "LATENCY TOLERANT DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER", <u>US Patent Application Ser. No. 10/643,585</u> , filed August 18, 2003 (1376.700US1), 17 Pages	
		SCOTT, S. L., et al., "RELAXED MEMORY CONSISTENCY MODEL", <u>US Patent Application Ser. No. 10/643,754</u> , filed August 18, 2003 (1376.724US1), 144 Pages	
		SHEETS, K., et al., "REMOTE-TRANSLATION MECHANISM FOR A MULTINODE SYSTEM", <u>US Patent Application Ser. No. 10/643,758</u> , filed August 18, 2003 (1376.729US1), 42 Pages	
		SHUMAY, M., "Deadlock-Free Packet Networks", <u>Transputer Research and Applications 2</u> , NATUG-2 Proceedings of the Second Conference of the North American Transputer Users Group, (October 18-19, 1989), 140-177	
		SNYDER, L., "Introduction to the Configurable, Highly Parallel Computer", <u>IEEE</u> , (January 1982), pp. 47--56	
		TALIA, D., "Message-Routing Systems for Transputer-Based Multicomputer", <u>IEEE Micro</u> , Vol. 13, No. 3, XP000380340, (June 1993), 62-72	
		WANG, WEILIN, et al., "Trunk Congestion Control in Heterogeneous Circuit Switched Networks", <u>IEEE</u> , (July 1992), pgs. 1156-1161	
		WU, MIN-YOU, et al., "DO and FORALL: Temporal and Spatial Control Structures", <u>Proceedings, Third Workshop on Compilers for Parallel Computers</u> , ACPC/TR, July 1992,	
		YANG, C. S., et al., "Performance Evaluation of Multicast Wormhole Routing in 2D-Torus Multicomputers", <u>IEEE</u> , (1992), 173-178	
		YANTCHEV, J., et al., "Adaptive, low latency, deadlock-free packet routing for networks of processors", <u>IEEE Proceedings</u> , 136, (May 1989), pp. 178-186	

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